A Comparative Study on TiO_2 and SiO_x Dielectric based MOS Capacitance

Ashik Some[1], Diksha Barnwal[1], Arnab Shome[1], Birojit Chakma[1], Lalaram Arya[1], B.S. Thoma[1], Aniruddha Mondal[1]

[1]*Dept. of Electronics & Communication Engineering, NIT Agartala, Jirania, Tripura, 799046*

ABSTRACT

The TiO_2 and SiO_x dielectric based n-MOS and p-MOS devices were fabricated by using e-beam evaporation technique on Si <100> substrates (33.5 Ωcm for n-Si and 30 Ωcm for p-Si). The TiO_2 and SiO_x (99.999% pure, MTI USA) have been evaporated to fabricate the 50 nm thin films (TF) on the Si substrates. The deposition rate was kept constant at 1.2 A^o/s for both TiO_2 and SiO_x material. The upper electrodes of diameter 1.5 mm were made of silver (Ag) and aluminium (Al) metal on TiO_2 and SiO_x thin film (TF) respectively. The Capacitance-Voltage (C-V) measurements were carried out on the TiO_2 and SiO_x based MOS devices using LCR meter (HIOKI, 3532-50). The maximum accumulation capacitance of 7.4 pF and 6.5 pF were measured for TiO_2 based n-MOS and p-MOS respectively at 1 MHz. The carrier concentration of $5.9 \times 10^{18}/m^3$ for n-Si/TiO_2 TF/Ag device and 1.29×10^{21} $/m^3$ for p-Si/TiO_2 TF/Ag device were calculated. The accumulation capacitance of 5.0 pF was measured for SiO_x based p-MOS device and the carrier concentration was measured 1.5×10^{19} $/m^3$. Finally, compared to SiO_x MOS device the TiO_2 based MOS device has larger capacitance, which may reduce the device leakage current. Therefore, the TiO_2 based high dielectric material may allow the device shrinking process for the fabrication of modern devices.

Keywords: MOS, TF, Schottky Contact, Ohmic Contact, TiO_2, SiO_x

1. INTRODUCTION

With the advancement in technology, the downscaling of devices is increasing the leakage current [1] and with continuing decrease of the gate dielectric thickness in conventional silicon MOS devices. The thin dielectric layer reduces the V_{th} which results in an increase of leakage current [2]. The simple relationship between the thickness of dielectric (d) and oxide capacitance (C_{ox}),

$$d= \varepsilon A/C_{ox} \quad (1)$$

does not hold for thin oxides. Lot of techniques have been employed to reduce the device leakage current [3,4]. A common technique of using high dielectric thin oxide increases the capacitance and

hence decreases the leakage current. The Schottky contact on the high dielectric oxide layer again decreases the leakage current compared to Ohmic contact [5]. In case of thin oxide layer, it is very difficult to measure the device capacitance at lower frequencies due to presence of noise [6]. Therefore, the higher frequencies are preferable to characterize the thin oxide layer based MOS devices. Also, Capacitance (C)–Voltage (V) measurement technique is a powerful technique to find out the MOS device quality for further improvements. This aforementioned method can be used to calculate the important parameters like carrier concentration (N_b), flat band voltage (V_{fb}) as well as other parameters easily.

In this report we have fabricated the n-MOS and p-MOS devices by using high dielectric TiO_2 and low dielectric SiO_x oxide layer as gate oxide on Si substrate. The contacts were made Ohmic for i) n-Si/SiO_x TF/Al contact (p-MOS), and Schottky for ii) n-Si/TiO_2 TF/Ag contact (p-MOS), iii) p-Si/TiO_2 TF/Ag contact(n-MOS) devices. The use of Schottky contact based devices lead to decrease in leakage current compared to Ohmic contact devices in which tunneling occurs [7,8]. The room temperature C-V was measured for the devices and compared. The flat band voltages (V_{fb}) and carrier concentration (N_b) were also calculated.

2. EXPERIMENTAL SECTION

The MOS devices were fabricated on 1cm×1cm cleaned p-type and n-type Si<100>substrate inside e-beam evaporator at a base pressure of 10^{-5}mbar. High purity TiO_2 TF and SiO_x TF (99.999% pure, MTI USA) of thickness 50 nm were deposited separately on two substrates n-Si and p-Si at a constant deposition rate of 1.1-1.2 Å/s. Silver (Ag) and Aluminum (Al) are deposited as the gate electrode through Aluminium (Al) mask hole, having an area of 1.77×10^{-6} m^2 on TiO_2 TF and SiO_x TF respectively. The capacitance through the devices were measured by using LCR meter (HIOKI, 3532-50).The carrier concentration was calculated from $1/C^2$ v/s V graph and flat band voltage (V_{fb}) obtained directly from C-V curve.

3. RESULTS AND DISCUSSIONS

Fig. 1 shows the graphs of C-V measurement for the three fabricated MOS devices done at frequency 1MHz at room temperature with the help of LCR meter (HIOKI, 3532-50). It can be seen from C-V curves of 50nm TF (Fig. 1) that the measured capacitance is dependent on both frequency and bias voltage. Each curve has three different regions of accumulation, depletion and inversion with a considerable shifting of voltage axis towards the negative bias due to the presence of interface states which is in equilibrium with semiconductor [9]. AC measuring signal frequency (1 MHz) is so high that the inversion layer charge Q_i cannot follow high frequency (HF) variation w.r.t changes in gate voltage (V_g) and thus assumed to be constant for a given DC bias [10]. The gate capacitance (C_g) in inversion at HF becomes

$$C_g = \left(\frac{1}{C_{ox}} + \frac{X_{dm}}{\varepsilon_o \varepsilon_r}\right)^{-1}. \quad (2)$$

C_g given by this equation is C_{min} at HF. The flatband (V_{fb}) voltages shown in the graphs have been calculated by using equations Debye length,

$$\lambda_D = \sqrt{\frac{\varepsilon_s kT}{q^2 N_b}} \quad (3)$$

and flatband capacitance,

$$C_{FB} = \frac{C_{ox}\varepsilon_s A/\lambda_D}{C_{ox}+\varepsilon_s A/\lambda_D} \quad (4)$$

Where N_b is the calculated carrier concentration [11], shown in Table1.

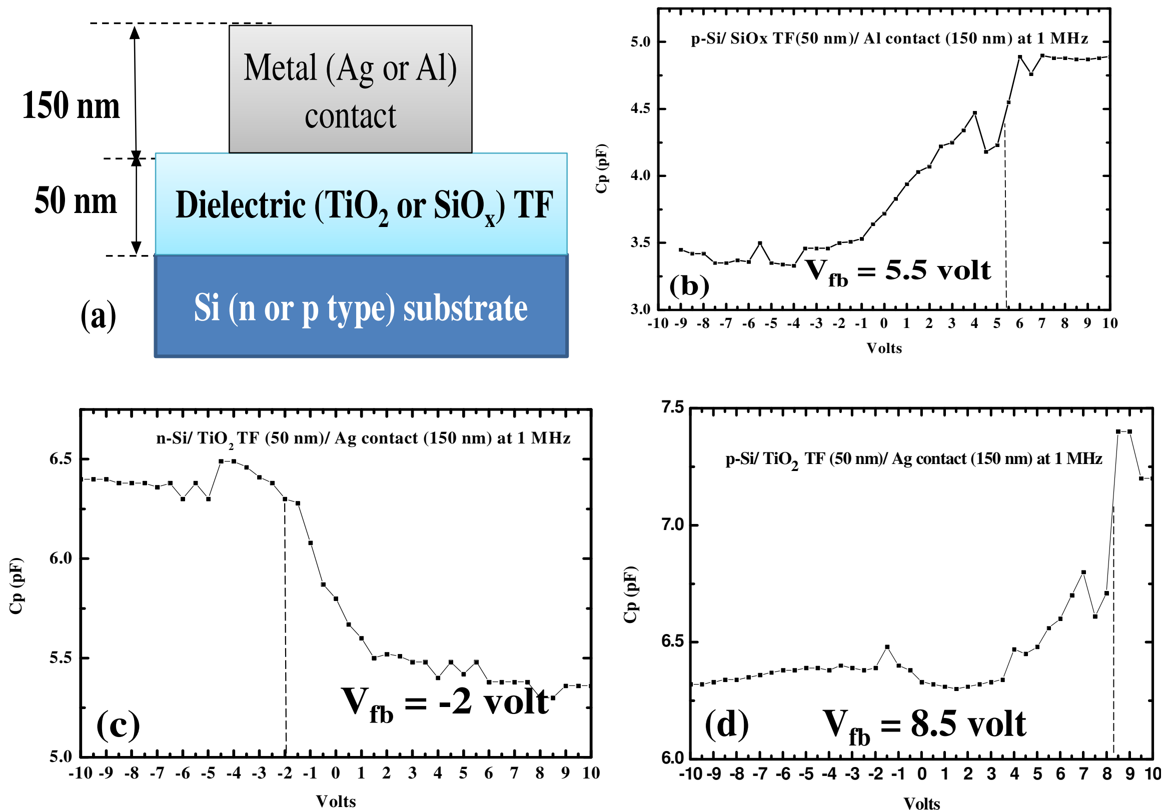

Fig. 1. a) Schematic diagram of fabricated MOS device. Capacitance versus voltage characteristics at 1MHz frequency for b) n-Si/SiOx TF/Al contact (p-MOS), c) n-Si/TiO_2 TF/Ag contact (p-MOS), d) p-Si/TiO_2 TF/Ag contact (n-MOS)

Fig. 2 shows the $1/C^2$ v/s V characteristics. These characteristics have been used to find the carrier concentration. The concentration (N_b) is given by

$$N_b = \frac{2}{e \times \varepsilon_r \times \varepsilon_o \times m} \tag{5}$$

where the dielectric permittivity (ε_r) of SiO_x is 3.9 and of TiO_2 is 80 [12] and m is the slope obtained from $1/C^2$ v/s V characteristics graphs. Three readings of N_b are obtained for three different values of slopes and their average is done to obtain final values for each graph.

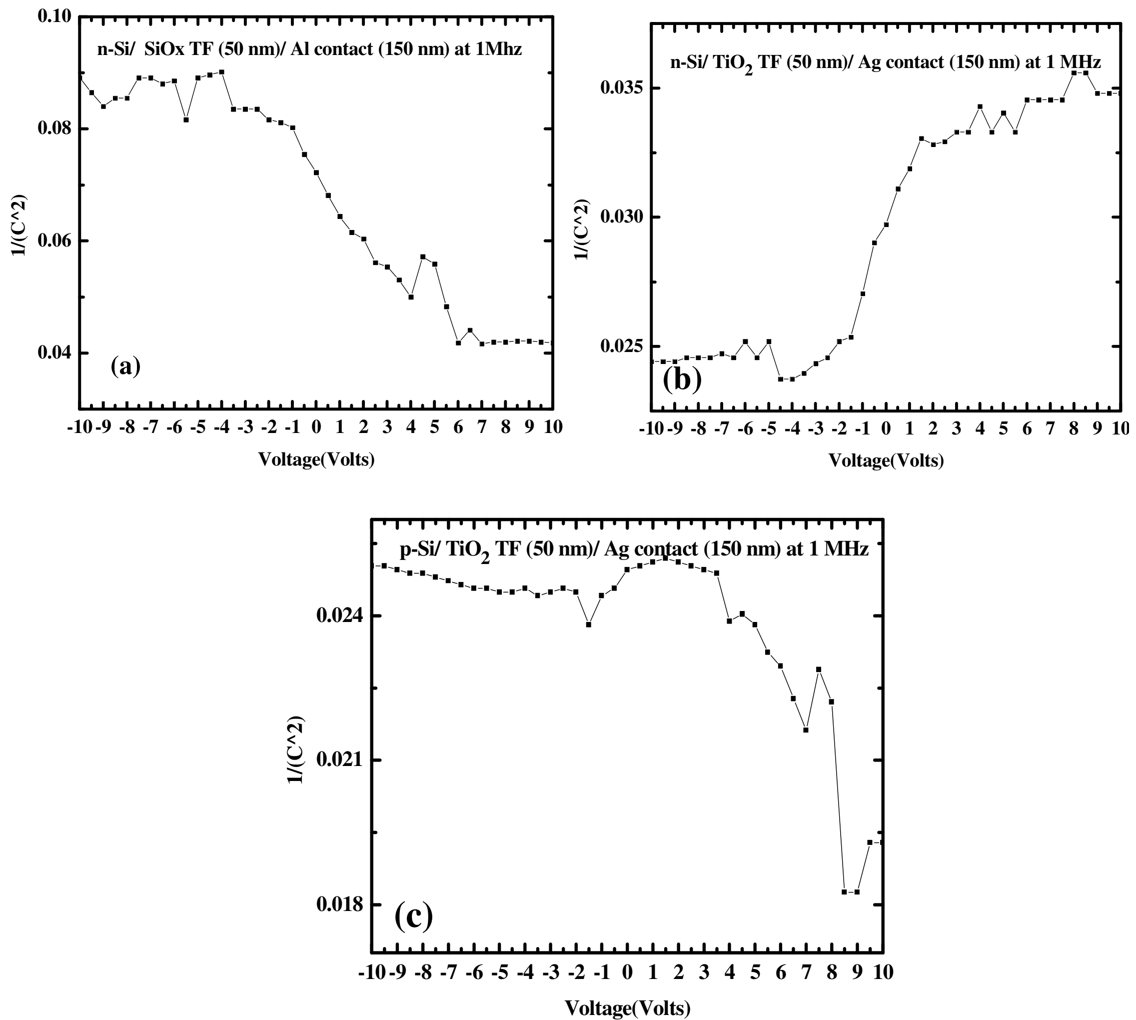

Fig. 2. $1/C^2$ v/s V characteristics graphs at 1MHz frequency for a) n-Si/SiOx TF/Al contact (p-MOS), b) n-Si/TiO_2 TF/Ag contact (p-MOS), c) p-Si/TiO_2 TF/Ag contact (n-MOS)

From $1/C^2$ v/s V characteristics, the obtained concentration of carriers is mentioned in the Table1.

Type	Concentration[/ m^3]	V_{fb} from graph [volts]	Flatband Capacitance, C_{fb} [pF]
p-Si/TiO_2 TF/Ag contact (n-MOS)	1.37×10^{19}	8.5	7.27
n-Si/TiO_2 TF/Ag contact (p-MOS)	6.26×10^{18}	-2	6.26
n-Si/SiOx TF/Al contact (p-MOS)	1.56×10^{19}	5.5	4.6

Table 1.Comparison of concentration, V_{fb} for a) p-Si/TiO_2 TF/Ag contact (n-MOS), b) n-Si/TiO_2 TF/Ag contact (p-MOS), c) n-Si/SiOx TF/Al contact (p-MOS)

4. CONCLUSION

The effect of introducing a high-k dielectric material (TiO_2) with a Schottky contact w.r.t a low-k dielectric material (SiO_x) with an Ohmic contact has been studied. The presence of Schottky contact reduces the tunneling and high-k dielectric is used to increase the value of capacitance thus allowing shrinking of device with minimum leakage current and an increase in capacitance as observed in C-V characteristics resulted in increased switching time.

5. ACKNOWLEDGEMENT

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