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ZVS Flyback Converter with Isolated and Non-isolated Outputs

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Abstract: ***The advancement of semiconductor technology lead to the requirement of multi-output dc-dc converter. The basic principle, analysis and design of a new topology dc-dc converter having isolated and non isolated outputs are presented in this paper. The circuit comprises of two non-isolated outputs having same ground and one isolated output on a second secondary. The switching pattern for the converter devices is generated using TMS320F28335 digital controller. The voltage stress on the primary switches of this converter is low and the regulation switch for auxiliary output is used for achieving zero voltage switching (ZVS) over the entire load range. The validity of the proposed topology is confirmed by the simulation results, carried out using PSIM software, obtained for three outputs with 12V,100mA; 6.6V,0.7A; and 5V,1.2A for set top box application.***

Keywords: ***Multi-output, ZVS, flyback, synchronous switches, Isolated, Non-isolated***

1. INTRODUCTION

The requirement of multi-output power supplies with different output voltage levels and load capacities has an increasing trend due to the advancement of power semiconductor technology. Also, the Switched Mode Power Supply (SMPS) needs to provide tightly regulated multiple outputs. Many systems require switching power supplies to provide regulated and often isolated outputs. The use of DC-DC converters with several outputs, isolated and non-isolated, is often effective and economical in meeting the system requirements[5 -6]. A variety of DC-DC converter topologies having several outputs have been explained in [17 - 21]. Among the various topologies, the flyback converter topology offers improved performance over other converter topologies due to its simple structure, low cost and high efficiency [14 -16]. A multi-output Forward-flyback Converter has been described in detail with Secondary Side Post Regulation [5-7]. The advantages of design simplicity and high efficiency of forward converter and the less expensive feature of flyback design are incorporated in the new converter topology of [3, 5]. But, the efficiency of this topology is low due to the conduction losses. Among different post regulation methods, the Post Regulation on Secondary Side(SSPR) is the best choice because it provides tight regulation for all outputs which is described in [7-8]. A switching converter with MOSFET-Rectifier Post Regulators, combines the advantage of both SSPR and synchronous rectifier is explained in [11]. Due to the presence of single secondary winding [11-15], the disturbance of parasitic resistance and transformer leakage inductance has been reduced. Even though the converter offers reduced cost and tight post regulation, the efficiency is less due to the conduction losses. In order to reduce the conduction losses, a new multi-output forward topology has been described with ZVS post regulated Multi-output Forward Converter with Synchronous Switches is proposed in [4]. The use of more number of switches and increased cost reduces the efficiency [2 - 3] of this converter. So, to overcome the above problems, ZVS Multi-output Flyback converter has been explained in [1].

Many applications require isolated outputs which are explained in the conventional multi output converters. When the isolated outputs are present, only the main output can be tightly regulated and the auxiliary outputs are quasi regulated which will reduce the effectiveness of the converter [9 - 11]. So, the proposed converter uses both isolated and non isolated output using which the regulation can be carried out by controlling the switching devices.

This paper proposes a ZVS Flyback Converter which gives two non-isolated outputs and one isolated output. It has the advantages of both of the converter topologies.

2. OPERATION PRINCIPLE

A. Circuit Description

The proposed topology is a combination of both non-isolated and isolated outputs. The new topology is designed for three outputs. The converter circuit with three outputs is shown in Fig.1. The transformer has two secondary windings. From one secondary, two non-isolated outputs are derived and from the

other, an isolated output is taken. The converter circuit has two synchronous switches on one secondary with two outputs with a common ground. The primary switches Q_M,Q_A control the output voltage, V_{02} and the secondary side synchronous switches Q_{S2},Q_{S1} control the output voltage V_{01} i.e. in this converter both these outputs can be regulated. Synchronous switches replace the diodes to reduce the conduction losses. Hence, the efficiency will also be improved. The third output V_{03} will be quasi regulated by the primary switches.

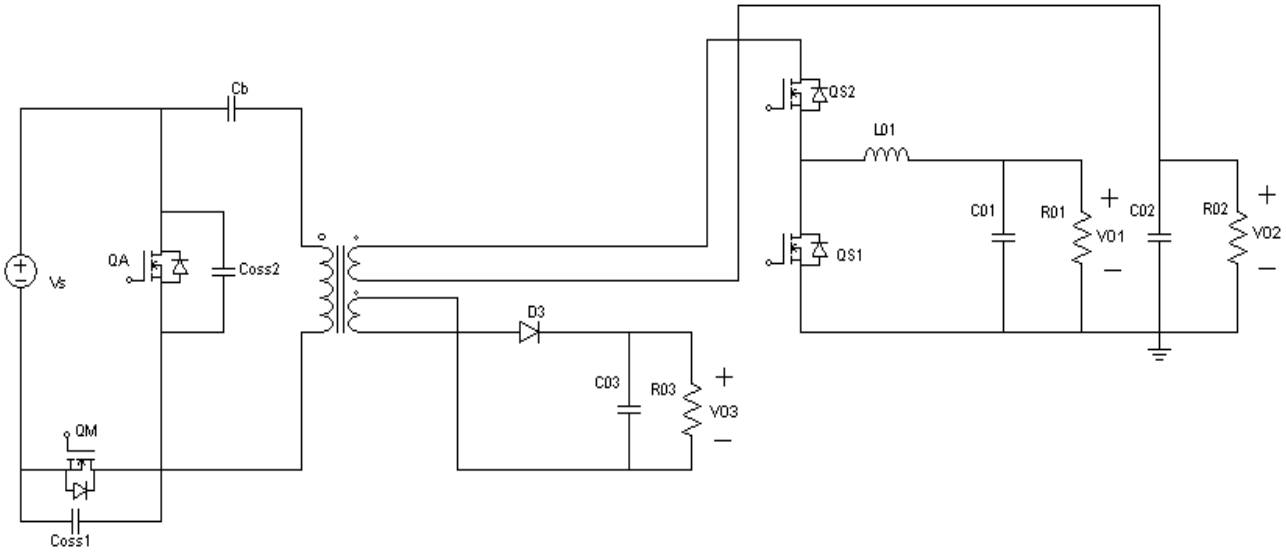


Fig.1. Proposed converter circuit diagram

For analyzing circuit behavior, assumptions made are as follows:

1) All device parasitic except those shown in Fig. 1, are neglected.

2) V_{Cb} the voltage across Cb, and the output voltages V_{01}, V_{02}, V_{03} does not change over a switching cycle

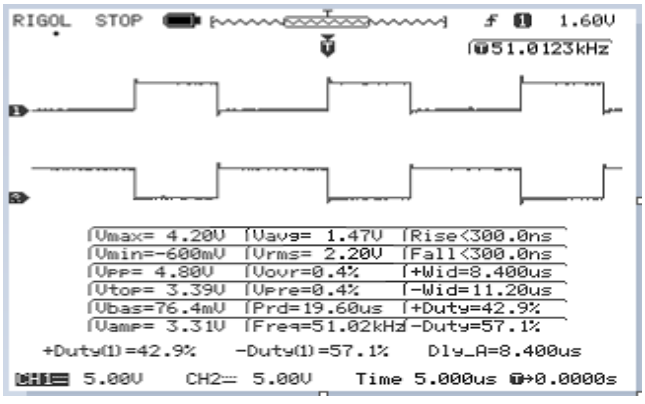
3) The main output voltage V_{02} is greater than auxiliary output voltages

4) The flyback transformer turns ratios are $n_1 = N_P / N_{S1}$ and $n_2 = N_P / N_{S2}$

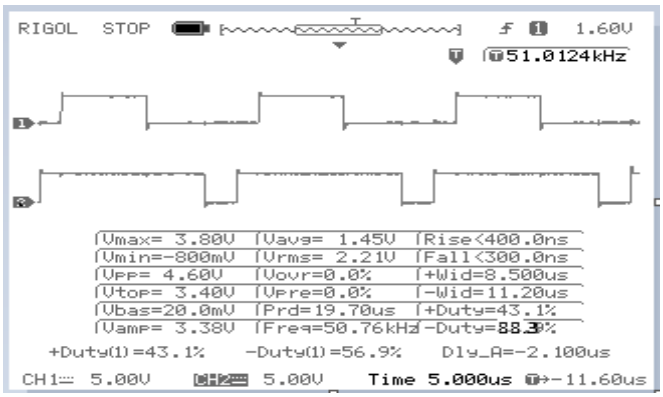
B. Pulse Generation using Digital Signal Controller

The pulses for the proposed converter topology have been generated using a Digital Signal Controller (DSC). The main objective is to process the data as quickly as possible to be able to generate an output stream of new data in real time. The TMS320F28xx and TMS320F28xxx are members of the C200 DSP generation used for embedded control applications. The converter topology uses TMS320F28335 processor having high central processing unit (32-Bit) performance with clock rate of 150MHZ.

The pulses generated from TMS320F28335 is shown in Fig.2. The primary switches Q_M and Q_A have been given complementary pulses with duty cycle 43% and 57% respectively, which is shown in Fig.2(a). Fig.2(b) shows the pulses for secondary side switches Q_{S2} and Q_{S1} is having 43% and 83% duty cycle. The output voltage of the pulses generated by the digital controller is below 4V. This voltage is not sufficient to drive the switches in the converter. So, the isolation and amplification of pulses has been carried out using Opto-Coupler (IC-TLP250).



(a)



(b)

Fig.2. Pulse pattern for switching devices using TMS320f28335

3. OPERATING MODES

The operation of the converter is explained in this section in six modes.

Mode 1 : $(t_0 - t_1)$

This mode activates when the secondary switch Q_{S1} is turned off. During this mode switches Q_M and Q_{S2} are ON and the diode D_3 is reverse biased. A voltage V_S-V_{CB} is applied to the transformer primary, so the magnetizing inductance current $i_{LM}(t)$ increases linearly with a positive slope. While the output inductor current $i_{L01,}$ flows through the switch Q_{S2} in the secondary side. The output V_{01} is now in powering mode.

Mode 2 : $(t_1 - t_2)$

In mode 2, the secondary switch Q_{S2} is switched off. Hence the output inductor current i_{L01} (t) flows through the body diode of $Q_{S1,}$ which ensures the freewheeling action of the output.

Mode 3: $(t_2 - t_3)$

When the main switch Q_M is turned off, this mode initiates. During this period, leakage inductor current i_{lkg} is assumed to be constant. So the parasitic capacitances C_{0SS1} and C_{0SS2} are linearly charged and discharged by $i_{lkg}(t)$. The voltage of switch Q_{S2} in the secondary side is decreased. ZVS of switches Q_A and Q_{S2} can be achieved once the primary voltage reaches - V_{CB}.

Mode 4 : $(t_3 - t_4)$

The main output V_{02} receives power directly from the primary side in this mode when switches Q_A and Q_{S2} are turned on at ZVS. The diode D_3 is forward biased during this flyback mode. The difference between voltages that reflected from secondary, nV_{02} and the blocking capacitor voltage, V_{CB} will be the voltage across primary side leakage inductor. The secondary transformer current is the current reflected from primary i.e. n ($i_{LM}(t)$ - $i_{lkg}(t)$). During this interval also, the output freewheels. The sum of currents $iL_{01}(t)$ and $i_{S2}(t)$ will be flowing through Q_{S1}.

Mode 5 : $(t_4 - t_5)$

The auxiliary switch Q_A is turned off, Q_M is already in off condition. The secondary switches Q_{S1} & Q_{S2} are ON during this interval. The parasitic capacitances C_{0SS2} and C_{0SS1} are linearly charges and discharges by $i_{lkg}(t)$. Freewheeling action of the output still continues.

Mode 6: $(t_5 - t_6)$

Main switch Q_M is turned on with ZVS. Leakage current $i_{lkg}(t)$ is increased as voltage (V_S - V_{CB}) + nV_{02} applied to the leakage inductance. Mode 6 ends when the switch Q_{S1} is turned OFF.

4. DESIGN AND ANALYSYS

The resonance in the circuit occurs only due to the presence of parasitic capacitance and transformer leakage inductance instead of any other additional tank circuit. The design formulae for resonance are given in equations (1) & (2). The resonance frequency is selected as thrice that of switching frequency and the resonant inductor and capacitor are designed accordingly.

$$\omega_r = \frac{1}{\sqrt{2 L_{lkg} C_{oss}}} \quad (1)$$

Impedance,

$$Z = \sqrt{\frac{L_{lkg}}{2 C_{oss}}} \quad (2)$$

Specifications the proposed converter considered for design are as tabulated in Table. 1

Table 1 Electrical Specifications

Serial No.	Description	Specification	
1	Input voltage	V_{min}	16.5V
		V_{max}	13.5V
2	Topology	Flyback	
3	Switchinh frequency f_S	50kHz	
4	D_{max}	40%	
5	Output power P_0	11.82W	
6	Output 1	6.6V/700mA	
7	Output 2	12V/100mA	
8	Output 3	5V/1.2A	

The flyback transformer can be designed as follows.

The output voltage,

$$\frac{N_P}{N_S} = \frac{V_{in\,min}\,D}{V_0(1-D)} \quad (3)$$

$$V_0 = \frac{(V_{in\,min}-1)(\frac{N_S}{N_P})}{(\frac{T}{T_{ON}})} - 1 \quad (4)$$

The primary inductance of the transformer is,

$$L_{pri} = \frac{(V_{DC}-1)V_{DC}\,T_{ON}^{\ 2}}{2.5\,P_0\,T} \quad (5)$$

Permeance

$$\Lambda = \frac{\mu_0\mu_r A_C}{l_m + \mu l_g} \quad (6)$$

Number of turns in the primary winding,

$$N_P = \sqrt{\frac{L_{pri}}{\Lambda}} \quad (7)$$

Turns ratios for secondary windings are,

$$n_1 = \frac{N_P}{N_{S1}} = \frac{V_{in\,min}\,D}{V_{S1}(1-D)} \quad (8)$$

$$n_2 = \frac{N_P}{N_{S2}} = \frac{V_{in\,min}\,D}{V_{S2}(1-D)} \quad (9)$$

The flyback transformer turns ratios can be found from equations (6),(7) & (8)

The output inductance,

$$L = \frac{V_0(1-D_{min})}{\Delta i_L . f_S} \quad (10)$$

Number of turns for the output inductor,

$$N = \sqrt{\frac{L}{\Lambda}} \quad (11)$$

Assuming an output voltage ripple of 1%, the output capacitance can be calculated using the equation (12).

$$\frac{\Delta V_0}{V_0} = \frac{D}{RCf} \quad (12)$$

The components used for the simulation are listed in Table. 2

TABLE.2 COMPONENTS LIST

Serial No.	Component Description	Specification
1	Switches (Q_M , Q_A, Q_{S2}, Q_{S1})	IRF540
2	Diode (D_3)	FR60 MIC
3	Leakage Inductance(L_{lkg})	7µH
4	Magnetizing Inductance (L_m)	1000µH
5	Transformer turns (N_P:N_{S1}:N_{S2})	1:2:1.5
6	Parasitic capacitances (C_{oss1} , C_{oss2})	200nF
7	Output capacitances (C_{01},C_{02},C_{03})	220µF
8	Clamping capacitance (C_B)	1µF
9	Output inductance (L_{01})	43µH

5. SIMULATION RESULTS AND DISCUSSIONS

A. Simulation without feedback

The proposed converter's performance has been verified using PSIM software. The multi-output topology includes two non-isolated and one isolated outputs. The simulation has been carried out for circuits with and without feedback loop. The results obtained (12V/100mA; 6.6V/0.7A; 5V/1.2A) for open loop simulation is shown as pictured in Fig.3 to Fig.5.

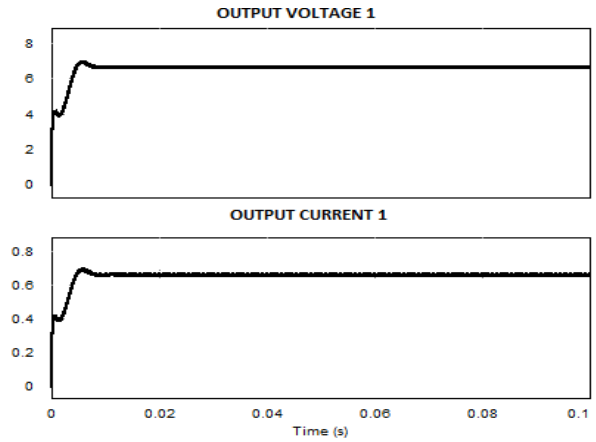


Fig.3. Waveforms for Output V_{01}

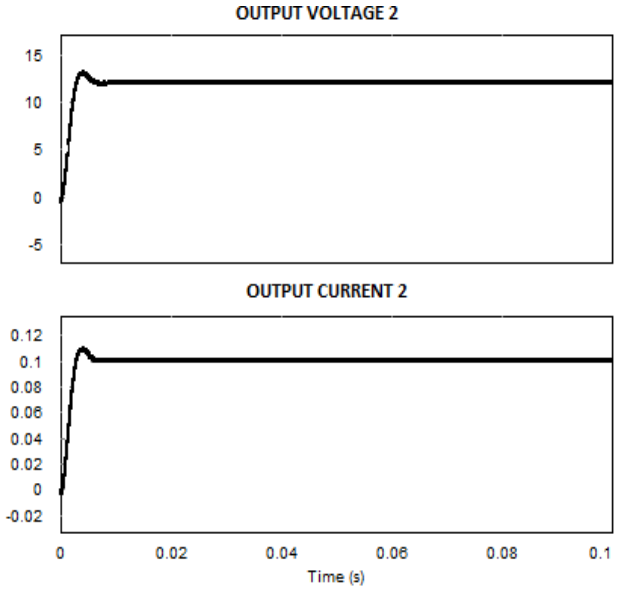


Fig.4. Waveforms for output V_{02}

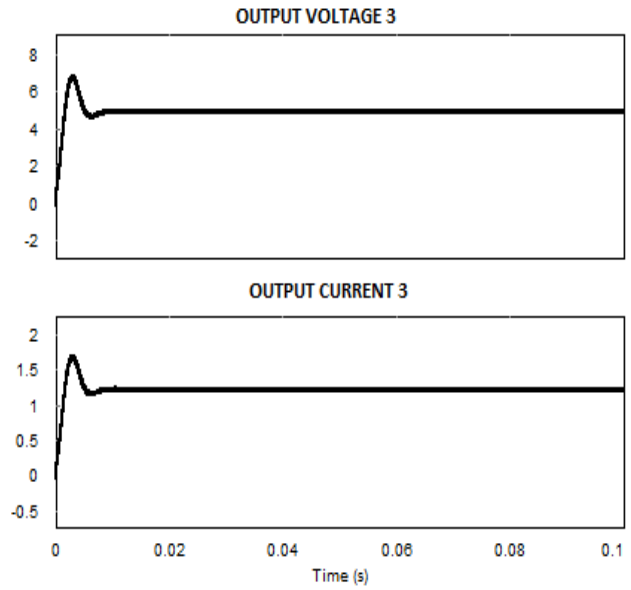


Fig.5. Waveforms for output V_{03}

Fig.3 shows the waveforms of voltage and current for output 1 with voltage 6.6V and current 700mA. Fig.4 shows the waveforms for output 2 with voltage 12V for a current of 100mA and that for output 3 is shown in Fig.5 with voltage 5V for a current of 1.2A.

B. Closed loop simulation

Regulated outputs are given out with closed loop control. The closed loop control diagram is shown in Fig.6. The output voltage is sensed and given to the controller. The pulses obtained are fed as the gating pulse for the switches.

The closed loop simulation is performed with PSIM software, main output voltage V_{02} is sensed and given to the controller. The pulses obtained is given to the primary switches. By controlling these switches, main output V_{02} can be regulated.

The results obtained for closed loop simulation is shown from Fig.7 to Fig.9. From the simulation results of V_{02}, it can be observed that the main output voltage is controlled for a load variation of 20%. The voltage and current before load variation are 12V & 100mA and that after load variation is 12.02V & 83mA, which is tolerant.

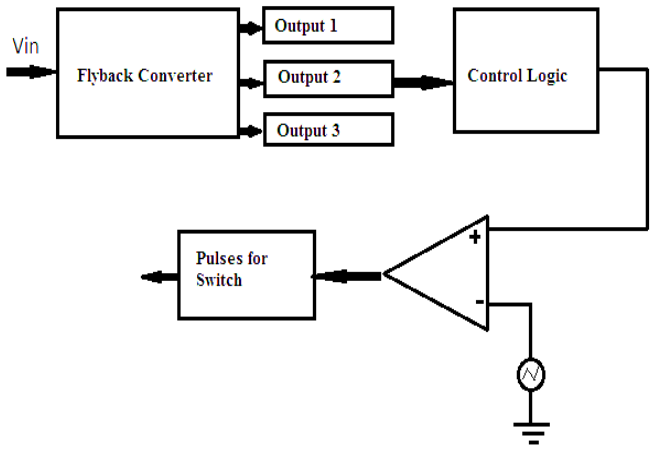


Fig.6. Closed loop control diagram

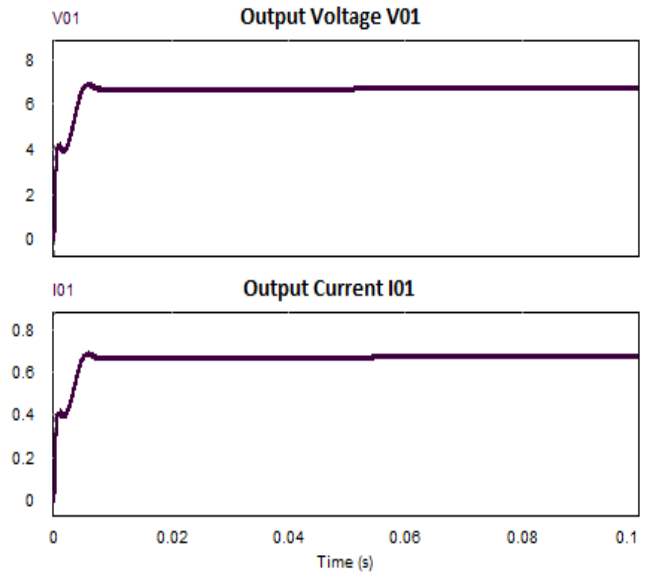


Fig.7. Results for circuit with feedback at output-1

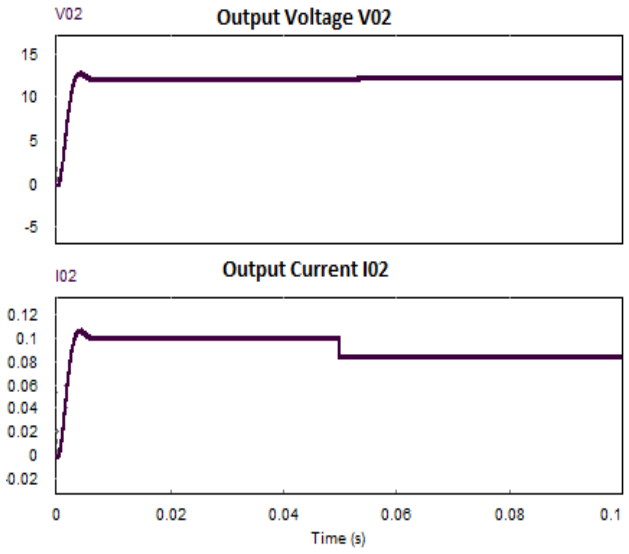


Fig.8. Results for circuit with feedback at output-2

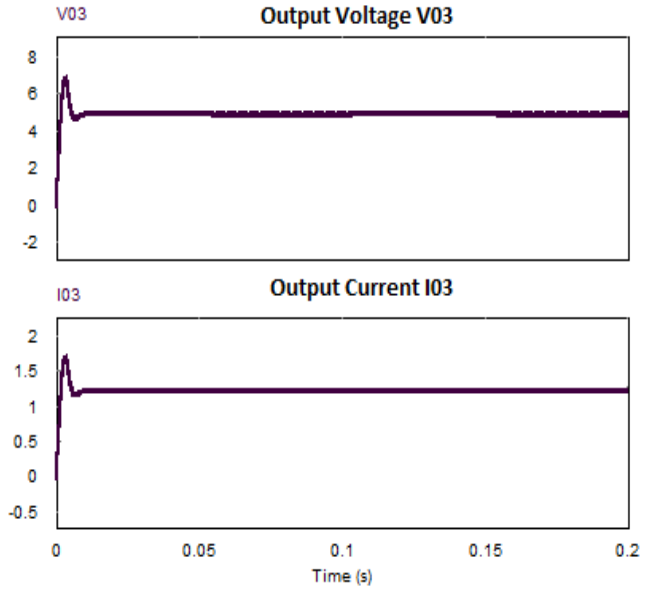


Fig.9. Results for circuit with feedback at output-3

6. SOFT SWITCHING

The present day converters use kHz to diminish the size of the filter components. But, due to the increase in junction temperature, the switching losses are very high. So, in order to decrease the switch losses and Electro Magnetic Interference (EMI) soft switching technique is used. The ZVS during turn ON and ZCS during turn OFF of the converter switches are revealed in Fig. 10 to 12. Due to the achievement of soft switching, the driving and switching losses are reduced.

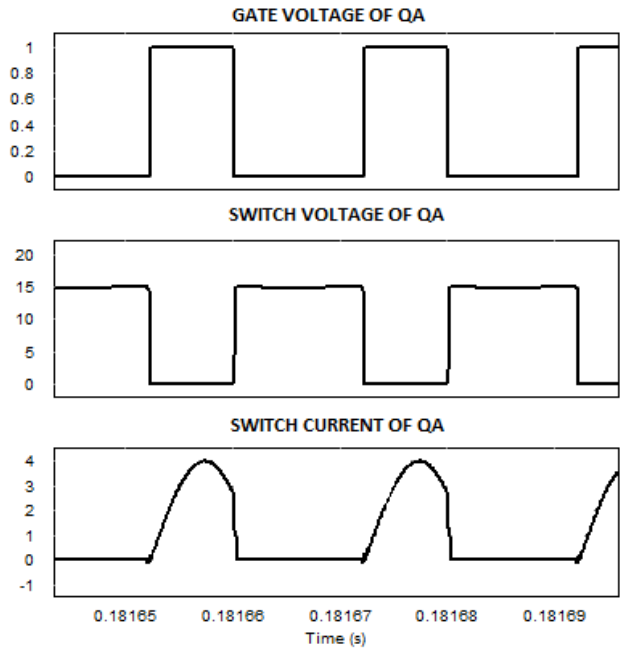


Fig.10. ZVS Waveform of Switch Q_A

From Fig. 10, it is clear that ZVS is achieved during turn ON and turn OFF of switch Q_A, switch voltage of Q_A is brought to zero before gate voltage is applied or removed. ZVS during turn ON and ZCS during turn OFF is achieved in switch Q_M as shown in Fig.11. And ZVS waveform for switch Q_{S1} is shown in Fig.12.

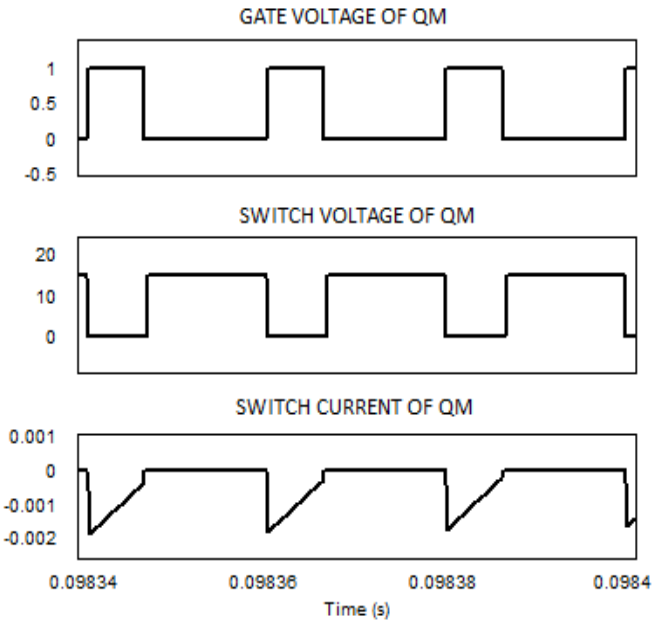


Fig.11. ZVS Waveform of Switch QM

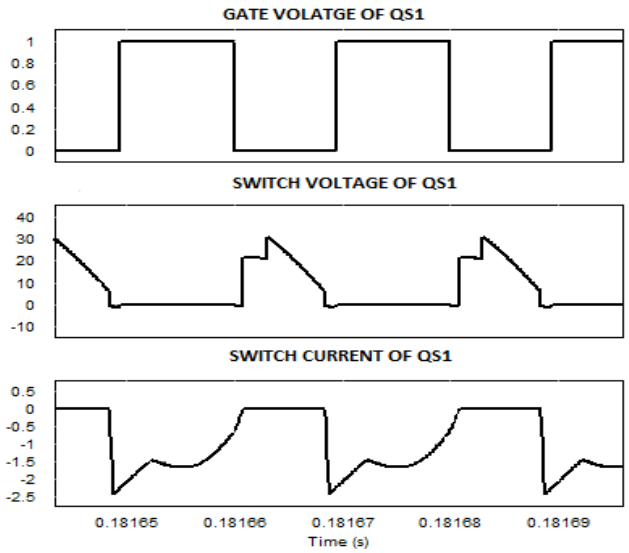


Fig.12. ZVS Waveform of Switch QS1

7. CONCLUSIONS

Multi-output power supplies with different output voltage levels and load capacities having tight regulation is desired for different applications in electronics industry. The effectiveness of the converter is increased due to the presence of tightly regulated both isolated and non-isolated outputs, which is absent in the conventional converter topology. A Zero-Voltage Switching (ZVS) Flyback Converter with isolated and non-isolated outputs is designed and simulated using PSIM software. From the simulation results, three outputs 12V,100mA; 6.6V,0.7A; and 5V,1.2A are obtained for an input of 15V. These outputs of the converter topology can be used for applications such as set top boxes, small DVD players and decoders, industrial and communications applications using Field Programmable Gate Arrays and complex logic chips. The pulses for the proposed converter topology have been generated using TMS320F28335 digital controller and the experimental confirmation of the proposed topology can be carried out using this digital controller. The topology can also be used for the design of more number of isolated and non-isolated outputs.

REFERENCES

[1] Jae-Kuk Kim,Jeong-Eon Park,Duk-You Kim and Gun Woo Moon, "Zero-Voltage-Switching Multi Output Flyback Converter With Synchronous Switches," 8th International Conf. on Power Electronics, 2011, pp. 868-875.

[2] W.J.Lee, S.W. Choi, C. E. Kim, G. W. Moon, "A New PWM-Controlled Quasi-Resonant Converter for a High Efficiency PDP sustaining Power Module ", IEEE Trans. Of Power Electronics, vol.23, 4, 2008, pp. 1782-1790.

[3] Jang, Jovanovic, and Dilman, "Light-Load Efficiency Optimization Method", Proceeding IEEE conf., 2009, pp. 1138-1144.

[4] J. K. Kim, S. W. Choi & G. W. Moon, " Zero-Voltage-Switching-Post-Regulation Scheme for Multi-output Forward Converter with Synchronous Switches", Proc. IEEE ECCE Conf., 2009, pp. 668-675.

[5] Deepti.T., Deepa.K & VijayaKumar, "Implementation & comparison of a new moc with post regulators ",5TH India International Conf. on Power Electronics, 2012, pp. 1-5

[6] Deepa.K, Padmaja.P.J & VijayaKumar, "PWM-Closed-Loop Controlled-Multi-Output Push Pull Converter", International Conference on Control Communication and Computing , IEEE, 2013, pp.426– 430.

[7] Y. He, Y. Gu, H. Chen, & Z. Qian, " Novel-Multi-Output-Forward flyback Converter With Secondary Side Post Regulation ", Proc. IEEE Conf., 2004, pp.618-621.

[8] Chen, " Small Signal Analysis of a Synchronous Switch Post Regulator with Coupled Inductors ", IEEE Trans. Ind. Electron., vol.47, no. 1, 2000, pp. 55-66.

[9] K.Deepa, M.VijayaKumar ," ZVS Multi Output Push Pull QRC Using Analog Controller IC UC3825 for Low Power Applications", second American Applied Science Research Conference on Power & Energy Systems, to be published in AASRI Procedia, Elsevier publication 2013.

[10] K.Deepa, R.Jeyanthi,Vijaya Kumar.M, "Analysis of a Quasi - Resonant Switch Mode Power Supply for Low Voltage Applications", ACEEE International Journal on Electrical and Power Engineering, vol..4, Issue No.2, Aug 2013, pp.85 to 92.

[11] Yao, Hong Mao, Liu, &. Batarseh, " Zero-Voltage-Switching-Buck-Flyback Isolated DC-DC Converter with Synchronous Rectification", Proc. of IEEE Conf., 2006, pp. 545-550.

[12] Yao, Mao, Liu, & Batarseh, " Zero-Voltage-Switching-Buck-Flyback Isolated DC-DC Converter with Synchronous Rectification ", Proc. IEEE Conf., 2006, pp.545-550.

[13] Mullett, Cathell, "Improving the Regulation of Multi-Output Flyback Converters" , Applied Power Electronics Conference and Expo, APEC 2009. 24th Annual IEEE, pp. 1923 – 1926.

[14] K. Deepa, Sanitha Mary Kurian., M.VijayaKumar, "Active-Clamp Zero Voltage Switching Multiple Output Flyback Converter with Voltage Doubler", International Review on modelling & simulation, Vol.6, 2013, pp. 351– 359.

[15] Deepa.K, HridyaMerinSaju & M.Vijaya Kumar., "Soft Switched Flyback Converter For SMPS Applications", An International Conf. on Control Communication & Computing IEEE, 2013, pp. 475 – 478.

[16] Coruh, Urgun and Erfidan, "Design & implementation of flyback converters", Industrial Electronics & Applications, 5th IEEE Conference, 2010, pp. 1189 – 1193.

[17] Werner. J, Oliveira. S.V.G and Peres, A, "Design & implementation of a DC-DC flyback converter to feed a class a tube amplifier," Power Electronics Conference, 2011, pp. 992 – 996.

[18] Abraham I Pressman, "Switching Power Supply Design," 2nd edition, McGraw Hill publishers.

[19] L.Umanand, "Power Electronics essentials and applications", Wiley Publications, 1st Edition- 2009.

[20] Ned Mohan, "Power electronics-Converters-Applications & Design," Wiley Publications, 2nd Edition- 1995.

[21] Muhammad.S. Rashid, "Power Electronics Circuits Devices and Applications," 3rd edition, 2004.